MCA15

NEW SCHEME

USN

First Semester M.C.A Degree Examination, July / August 2003

Master of Computer Applications

(New Scheme)

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. Assume suitable data.

1. (a) Explain the different functional units of a digital computer with a neat diagram. **(7 Marks)**

(b) List the steps needed to execute the machine instruction ADD LOCA, RO in terms of transfers between the components processor and memory. Assume that the instruction itself is stored in the memory location INSTR. **(7 Marks)**

(c) What is a bus ? How choice of bus affects the performance of a computer ? **(6 Marks)**

2. (a) Explain the following
i) Byte - addressability
ii) Big - endian assignment
iii) Word - alignment **(6 Marks)**

(b) What are assembler directives ? Explain any two directives. **(4 Marks)**

(c) What is an addressing mode ? Explain different addressing modes. **(10 Marks)**

3. (a) Explain MMX instruction of IA32. **(4 Marks)**

(b) Explain the working of a static RAMcell and compare SRAM, with DRAM. **(10 Marks)**

(c) Give register structure of IA32. **(6 Marks)**

4. (a) What is bus arbitration ? Explain two approaches to bus arbitration. **(10 Marks)**

(b) Explain synchronous bus with a neat diagram. **(5 Marks)**

(c) What are interrupts ? Explain any one method for handling multiple devices. **(5 Marks)**

5. (a) Explain any two cache mapping functions. **(8 Marks)**

(b) Explain with a timing diagram how write and read operation takes place in 1k x1 memory chips. **(6 Marks)**

(c) Explain different types of ROM. **(6 Marks)**

6. (a) Describe BOOTH's algorithm for multiplication of two signed integers. Show an example. **(10 Marks)**

(b) Explain carry - look ahead adder. Write the number of gate delays required to perform n bit addition using ripple carry adder and carry - look ahead adder. **(10 Marks)**

Contd.... 2

7. (a) Explain three bus organisation of the data path with a neat diagram and write the control sequence for the instruction ADD R_4, R_5, R_6 for the three-bus organisation. **(10 Marks)**

   (b) Write a note on IEEE floating point standard. **(4 Marks)**

   (c) Explain hardwired control. **(6 Marks)**

8. Write short notes on :

   a) Daisy chain

   b) Optical disk

   c) Indirect Addressing

   d) DMA **(4×5=20 Marks)**

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MCA15

Reg. No.

First Semester M.C.A Degree Examination, January/February 2003

Master of Computer Applications (New Scheme)

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All questions carry equal marks.

1. (a) Explain the different functional units of a digital computer. **(6 Marks)**

(b) Highlight the developments made during different generations of computer. **(8 Marks)**

(c) What is a bus? Explain single bus structure in an architecture. **(6 Marks)**

2. (a) Explain the following :
i) Byte addressability
ii) Big-eudian assignment
iii) Little - eudian assignment. **(6 Marks)**

(b) What is an addressing mode? Explain different addressing modes. **(10 Marks)**

(c) What are assembler directives? Explain any two directives. **(4 Marks)**

3. (a) Explain the register structure of IA32 with a neat diagram. **(10 Marks)**

(b) Explain MMX instruction of IA32. **(4 Marks)**

(c) With a neat diagram explain how basic I/o operations take place. **(6 Marks)**

4. (a) What are interrupts? Explain any two methods for handling multiple devices. **(6 Marks)**

(b) What is bus arbitration? Explain two approaches to handle bus arbitration. **(8 Marks)**

(c) Explain synchronous bus structure with timing diagram. **(6 Marks)**

5. (a) Explain with a neat diagram how write and read operations take place in $1K \times 1$ memory chip. **(7 Marks)**

(b) Explain any two cache mapping functions. **(8 Marks)**

(c) Explain the working of a static RAM cell. **(5 Marks)**

6. (a) Explain Booth's algorithm to multiply two signed integers. Illustrate with an example. **(10 Marks)**

(b) With a neat diagram explain floating point addition/ subtraction unit. **(10 Marks)**

7. (a) Explain the microprogrammed control unit and compare it with hardwired control unit. **(10 Marks)**

(b) Explain three bus organization of the data path with a neat diagram and write the control sequence for the instruction. Add R_4, R_5, R_6 for the three bus organisation. **(10 Marks)**

8. Write short notes on :
i) ROMs
ii) IEEE floating point standard
iii) Multiprocessors and multicomputers
iv) Memory interleaving. **(20 Marks)**

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NEW SCHEME

MCA15

USN

First Semester M.C.A Degree Examination, January / February 2004

Master of Computer Applications

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All question carry equal marks.

1. (a) Define the following terms

i) Processor clock ii) RISC
iii) Complier iv) RAM v) Control unit

(10 Marks)

(b) Represent the decimal values 5, -2 and -10 in the following binary formats

i) Sign and magnitude
ii) 1st compliment
iii 2s compliment **(10 Marks)**

2. (a) Registers R_1 and R_2 of a computer contain the decimal value 1200 and 4600. What is EA of the memory operand in each of the following instructions?

i) Load $20(R_1), R_5$
ii) Move $\#3000, R_5$
iii) Store $R_5, 30(R_1, R_2)$
iv) Add $-(R_2), R_5$
v) Subtract $(R_1)+, R_5$ **(10 Marks)**

(b) Consider the following possibilities for saving the return address of a subroutine

i) In a processor register
ii) In a memory location
iii) On a stack

Which of these possibilities support subroutine resting and which support subrouting recursion **(10 Marks)**

3. (a) Explain IA-32 register structure and instruction format in detail **(12 Marks)**

(b) What is subroutine? Explain IA-32 subroutine with an example and show the stack details. **(8 Marks)**

4. (a) What is interrupt? Discuss polling and vectored interrupts. **(10 Marks)**

(b) Explain the DMA controller in detail. **(10 Marks)**

5. (a) Explain the internal organization of a 16×8 memory chip. **(10 Marks)**

(b) Discuss synchronous DRAM with its block diagram. **(10 Marks)**

6. Given two numbers A = 1101, B = 1011, multiply both the numbers using manual multiplication algorithm and show the array implementation. Compare it with binary multiplier. **(20 Marks)**

Contd.... 2

7. (a) Discuss the timing diagram of a READ operation in detail. **(10 Marks)**

(b) With an example discuss the microprogram sequencing. **(10 Marks)**

8. Write short notes on: **(20 Marks)**

i) Optical disks

ii) Booth Algorithm

iii) SRAMs

iv) ROMs

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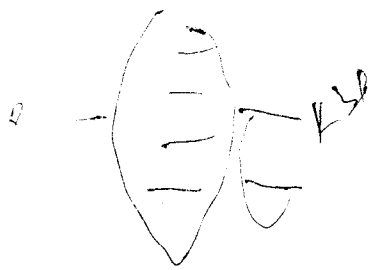

MCA15

NEW SCHEME

USN | | | | | | | | | | |

First Semester M.C.A Degree Examination, July/August 2004

Master of Computer Applications

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All question carry equal marks.
3. Write truth tables, block diagram wherever required.

1. (a) Explain different functional units of a digital computer. (8 Marks)
   (b) Differentiate between multicomputer and multiprocessor. (4 Marks)
   (c) With neat block diagram, explain the interconnected functional units of a single bus. (8 Marks)

2. (a) What is an addressing? Explain different addressing modes. (10 Marks)
   (b) Write an assembly language program to sort the N numbers. (10 Marks)

3. (a) Differentiate between memory mapped I/O and isolated I/O. (4 Marks)
   (b) Explain the program flow control with example. (10 Marks)
   (c) Give the register structure of IA-32 machine. (6 Marks)

4. (a) List and explain the sequence of steps that takes place when an interrupt is received by CPU. (12 Marks)
   (b) Explain how DMA transfer will improve the data transfer rate in a computer. (8 Marks)

5. (a) With a neat diagram explain how read and write operations are carried out in $1k \times 1$ memory chip. (10 Marks)
   (b) With neat diagram, explain the internal organization of a $2M \times 8$ dynamic memory chip. (10 Marks)

6. (a) Discuss the working of a 4-bit carry-look ahead adder. (7 Marks)
   (b) State and explain different types of ROM. (6 Marks)
   (c) Explain Booth's algorithm to multiply two signed numbers with example. (7 Marks)

7. (a) Explain the hard-wired control with the help of the neat block diagram and compare this with micro program control concept. (12 Marks)
   (b) Explain IEEE standards for floating point numbers. (6 Marks)

8. Write short notes on : (4×5=20 Marks)
   (a) Multimedia Extension (MMX) instructions
   (b) Assembler directives
   (c) Flash memory
   (d) Memory system concepts.

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NEW SCHEME

MCA15

USN

First Semester M.C.A Degree Examination, January / February 2005

Master of Computer Applications

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All question carry equal marks.
3. Write figures wherever necessary.

1. (a) Briefly discuss the different types of computers. **(6 Marks)**

(b) Explain the basic operational concept of a digital computer. **(10 Marks)**

(c) Explain the single bus structure. **(4 Marks)**

2. (a) Explain the different types of addressing modes with an example for each. **(12 Marks)**

(b) Explain the following :
i) Stack ii) Subroutine **(8 Marks)**

3. (a) Give register structure of IA-32 machine. **(6 Marks)**

(b) Discuss the different addressing modes of IA-32 machine. **(10 Marks)**

(c) Explain the following instructions with respect to IA-32 machine
i) LEA ii) JG iii) LOOP iv) SHL **(4 Marks)**

4. (a) What are the two different I/O techniques in which CPU is directly involved in data transfer? **(12 Marks)**

(b) With the block diagram of a DMA controller, explain how data is transferred between DISK and memory. **(8 Marks)**

5. (a) Show the organization of bit cells in a 16 x 8 memory chip and explain how read and write operations are carried out. **(10 Marks)**

(b) Explain memory hierarchy in digital computer. **(10 Marks)**

6. (a) Explain the working of a 4-bit carry-look-ahead adder. **(8 Marks)**

(b) Multiply 13 x (6) using 'Booths algorithm'. **(6 Marks)**

(c) Divide 1110 by 0011 using restoring technique. **(6 Marks)**

7. (a) Explain with the block diagram single bus organization of the data path inside a processor. **(12 Marks)**

(b) Write the control sequence for execution of the instruction ADD (R7), R8. **(8 Marks)**

8. (a) Write short notes on : **(5 x 4-20 Marks)**
i) IEEE standard for floating point numbers
ii) Assembler directives
iii) Cache memory
iv) Horizontal versus vertical micro instructions.

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MCA15

NEW SCHEME

First Semester M.C.A. Degree Examination, Dec.06/Jan. 07

Computer Organization

Time: 3 hrs.] [Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain the different functional units of a digital computer. **(08 Marks)**
b. Differentiate between multi computer and multiprocessor. **(04 Marks)**
c. What is a bus? Explain single bus structure in architecture. **(08 Marks)**

2 a. What is an addressing? Explain different addressing modes. **(08 Marks)**
b. Write an assembly language program to compute the dot product of two vectors. **(08 Marks)**
c. Explain the following : i) Big – endian assignment ii) Little - endian assignment **(04 Marks)**

3 a. Explain IA – 32 register structure and instruction format in detail. **(10 Marks)**
b. Write a IA – 32 program to read a line of characters and display it. **(06 Marks)**
c. Explain MMX instruction of IA – 32. **(04 Marks)**

4 a. What is bus arbitration? Explain two approaches to handle bus arbitration. **(08 Marks)**
b. Explain asynchronous bus structure with timing diagram. **(06 Marks)**
c. Write an ISR to read one line from a keyboard using interrupts on IA – 32 processors. **(06 Marks)**

5 a. Explain the Internal organization of a 2M × 8 dynamic memory chip. **(10 Marks)**
b. Explain with a neat diagram how write and read operations take place in 1k × 1 memory chip. **(10 Marks)**

6 a. Write short notes on i) FLASH memory ii) EPROM and EEPROM. **(06 Marks)**
b. State and explain IEEE standards for floating point numbers. **(06 Marks)**
c. Discuss on set associative – mapped cache organization. **(08 Marks)**

7 a. Explain Booth's algorithm to multiply two signed integers. Illustrate with an example. **(10 Marks)**
b. With a neat diagram explain floating point addition / subtraction unit. **(10 Marks)**

8 a. With a neat diagram explain the working of a micro programmed controller. **(06 Marks)**
b. Explain the bus organization of the data path with a neat diagram and write the control sequence for the instruction. Add R_4, R_5, R_6 for the three bus organization. **(08 Marks)**
c. Write the control sequence for the execution of the instruction:
Add (Rsrc), Rdst. **(06 Marks)**

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MCA15

USN

NEW SCHEME

First Semester MCA Degree Examination, July 2007

Computer Organization

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Differentiate between
   i) Primary and Secondary Memory.
   ii) Multiprocessors and Multi computers. **(06 Marks)**
   b. With neat block diagram , explain various functional units of a computer. **(10 Marks)**
   c. Explain the Single Bus Structure. **(04 Marks)**

2 a. Explain Zero address, One address, Two address and Three address instructions with an example for each. **(04 Marks)**
   b. Write an assembly language program to find sum of "N" numbers. **(06 Marks)**
   c. Register R_0 and R_1 of a computer contain the value 2200 and 2600. What is E_A of the memory operations in each of the following instructions?
   i) Load 10 (R_1), R_5
   ii) Store R_5, 30 (R_0, R_1)
   iii) Move (R_1), R_5.
   iv) Add - (R_0), R_5.
   v) Subtract (R_1) + R_5. **(10 Marks)**

3 a. Let the number of address lines and data lines be 20 and 16 respectively.
   i) Determine the memory capacity and word length of the processor.
   ii) Determine the range of address in Hexadecimal representation. **(08 Marks)**
   b. Explain the register structure of IA – 32 machine and their functions. **(08 Marks)**
   c. What are assembler directives? Explain any 2 of them. **(04 Marks)**

4 a. Explain DMA controller in detail. **(10 Marks)**
   b. What is Interrupt? Discuss polling and vectored interrupts. **(10 Marks)**

5 a. Describe the internal organization of a 2M $\times$ 8 dynamic memory chip. **(10 Marks)**
   b. With the help of suitable diagram, explain how mapping is performed in direct mapped cache organization. **(06 Marks)**
   c. With neat diagram, explain the memory interleaving concept. **(04 Marks)**

6 a. Discuss Booth Algorithm used for multiplication. **(10 Marks)**
   b. Explain integer division using restoring technique. **(06 Marks)**
   c. Write a note on IEEE standard for floating point numbers **(04 Marks)**

7 a. Discuss the timing diagram of a READ operation in detail. **(10 Marks)**
   b. Explain the basic organization of micro programmed control unit. **(10 Marks)**

8 Write short notes on :
   a. Big Endian and Little Endian assignments
   b. Risc and Cisc
   c. Multimedia extension (MMX) instructions.
   d. Memory mapped input output and Isolated input output. **(20 Marks)**

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MCA15

First Semester MCA Degree Examination, Dec. 07 / Jan. 08
Computer Organization

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Discuss the various generations through which the computers have evolved to present stage. Indicate the important technological features and devices that characterized each generation. **(10 Marks)**

b. Represent the decimal values 5, -2, -10, -3 and 14 as signed, 5-bit numbers in the following binary format i) Sign and magnitude ii) 2's complement. **(10 Marks)**

2 a. Write a program that can evaluate the expression $A \times B + C \times D$ in a single accumulator processor. Assume that processor has Load, Store, Multiply and Add instructions and all values fit in the accumulator. **(06 Marks)**

b. What is the difference between big endian and little endian format? **(06 Marks)**

c. Explain Arithmatic and Logical shift instructions. **(08 Marks)**

3 a. Explain IA-32 Register structure. **(12 Marks)**

b. Explain IA-32 Addressing Modes. **(08 Marks)**

4 a. What is bus arbitration? Explain distributed arbitration. **(10 Marks)**

b. What is interrupt latency? Show a circuit arrangement, where by several devices may interrupt processor on a single interrupt line on fixed priority basis and explain. **(10 Marks)**

5 a. Discuss synchronous DRAM's with neat block diagram. **(10 Marks)**

b. Explain set Associative and Associative mapping methods used in cache. **(10 Marks)**

6 a. Multiply two 5-bit numbers 01101 and 11010 using Booths algorithm. **(10 Marks)**

b. With neat figure of bit stage cell explain carry look-ahead addition. **(10 Marks)**

7 a. With neat figure explain multiple bus organization. **(10 Marks)**

b. List and explain the sequence of control steps required to execute instructions. Add (R_3), R_1. **(10 Marks)**

8 Write short notes on:

a. Pipelining and Superscalar Operation.

b. CMOS memory cell.

c. Big Endian and Little Endian assignments.

d. Multiprocessors and Multicomputers. **(20 Marks)**

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MCA15

First Semester MCA Degree Examination, June / July 08

Computer Organization

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. List the steps needed to execute the machine instruction. Add LOCA, RO in terms of transfer between the system component and some simple control commands. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC. **(10 Marks)**

b. Convert the pairs of decimal numbers: i) 5 and 10 ii) –14 and 11 to 5-bit, signed, 2's compliment binary numbers and add them. State whether or not overflow access in each case. **(10 Marks)**

2 a. Write a program that can evaluate the expression A×B + C×D in a single accumulator processor. Assume that the processor has Load, Store, Multiply and Add instructions, and that all values fit in the accumulator. **(10 Marks)**

b. Consider the following possibilities for saving the return address of a subroutine:
i) In a processor register
ii) In a memory location associated with the call
iii) On a stack.
Which of these possibilities supports subroutine nesting and which supports subroutine recursion. **(10 Marks)**

3 a. Which of the following IA-32 instructions would cause the assembler to issue a syntax error message? Why?
i) ADD EAX, EAX ii) ADD [EAX], [EBX + 4] iii) SUB EAX, [EBX + ESI * 4 + 20]
iv) SUB EAX, [EBX + ESI * 10] v) ADD EAX – 31728542 vi) MOV 20, EAX
vii) MOV EAX, [EBP + ESP * 4]. **(14 Marks)**

b. Explain IA-32 register structure in detail. **(06 Marks)**

4 a. List the differences between a subroutine and an interrupt – service routine. **(06 Marks)**

b. Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A/B is being serviced. Suggest different ways in which this can be accomplished in each of the following cases:
i) The computer has one interrupt request line
ii) Two interrupt request curves, INTR1 and INTR2, with INTR1 having higher priority.
Specify when and how interrupts are enabled and disabled in each case. **(14 Marks)**

5 a. Explain internal organization of memory chips. Give the organization of a 1 K × 1 memory chip. **(10 Marks)**

b. Give the memory organization of 8 m × 32 using 512 k × 8 memory chips. **(10 Marks)**

6 a. Discuss the memory interleaving, hit rate and miss penalty. **(06 Marks)**

b. Explain in detail the carry-lookahead addition. **(14 Marks)**

7 a. Multiply the following pair of signed 2's compliment numbers using the booth algorithm. A is the multiplicand and B is the multiplier. A = 010111 and B = 110110. **(10 Marks)**

b. Explain the floating-point operation using floating-point addition-subtraction unit. **(10 Marks)**

8 a. Explain multiple-bus organization and give the block diagram. **(10 Marks)**

b. Explain the microinstruction – sequencing organization. Give the block diagram. **(10 Marks)**

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USN | | | | | | | | | | |

07MCA13

First Semester MCA Degree Examination, Dec 08 / Jan 09
Fundamentals of Computer Organization

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Perform the following number convections : i) $(628)_{10} = (?)_2$ ii) $(AB2D)_{16} = (?)_{10}$ iii) $(455)_{10} = (?)_8$ iv) $(10011)_2 = (?)_{10}$ v) $(320)_8 = (?)_{10}$. **(10 Marks)**

b. Perform the subtractions using complements method.
i) $(11010)_2 - (10010)_2$ ii) $(101\ 011\ 00)_2 - (1001\ 00\ 11)_2$. **(04 Marks)**

c. Write the procedure for simplifying a Boolean expression using Karnaugh map. **(06 Marks)**

2 a. What is Bits, Bytes and Nibbles. **(06 Marks)**

b. What are Universal gates? Explain. **(06 Marks)**

c. State and prove De – Margan's theorem. **(08 Marks)**

3 a. What are the different types of computer? Explain briefly. **(10 Marks)**

b. Draw the block diagram of the functional view of a compute. Explain briefly. **(10 Marks)**

4 a. Explain Big – Indian and Little – Indian assignments for byte and word addressing with diagram. **(10 Marks)**

b. Explain the difference between indexed addressing and relative addressing modes with example. **(10 Marks)**

5 a. What is interrupt? Explain how multiple devices are handled in interrupts. **(10 Marks)**

b. What is bus arbitration? Explain two approaches to bus arbitration. **(10 Marks)**

6 a. Explain DMA with the help of block diagram. **(10 Marks)**

b. How mapping is done in direct mapped cache organization? Explain with diagram. **(06 Marks)**

c. What is memory interleaving? Explain with diagram. **(04 Marks)**

7 a. Explain i) Flash memory ii) EPROM iii) EEPROM. **(06 Marks)**

b. Explain Booth's Algorithm to multiply two signed numbers with example. **(10 Marks)**

c. Explain IEEE floating point standard. **(04 Marks)**

8 Write short notes on:
a. Half Adder.
b. Full Adder.
c. RISC and CISC.
d. MMX instructions. **(20 Marks)**

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07MCA13

First Semester MCA Degree Examination, Dec.09/Jan.10
Fundamentals of Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Perform the following number conversion
   i) $(123.12)_{10} = (?)_2$
   ii) $(123.12)_8 = (?)_{16}$
   iii) $(123.12)_{16} = (?)_{10}$
   iv) $(123.12)_{10} = (?)_8$
   v) $(123.12)_{16} = (?)_8$. **(10 Marks)**

   b. i) Construct a logic circuit using basic gates $Z = \overline{(A + B + \overline{C}\,D\,\overline{E})} + \overline{B}\,C\,\overline{D}$. **(05 Marks)**

   ii) Explain NOR gate and NAND gate with truth table, symbol and Boolean expression for each. **(05 Marks)**

2 a. What are the 2 forms of Boolean expressions? Explain with example. **(06 Marks)**

   b. Simplify the following expressions:
   i) $Z = ABC + A\overline{B} \cdot \overline{(\overline{A} \cdot \overline{C})}$ - using Boolean laws
   ii) $Z = \overline{C}\,(\overline{A}\,\overline{B}\,\overline{D} + D) + A\,\overline{B}\,C + \overline{D}$ - using K-map. **(06 Marks)**

   c. Explain binary addition-subtraction logic network, for signed numbers. **(08 Marks)**

3 a. Explain the basic operational concepts of a digital computer. **(10 Marks)**

   b. Explain the basic performance equation and tell how pipelining and superscalar operations improve the performance of a computer. **(10 Marks)**

4 a. Registers R_1 and R_2 of a computer contain the decimal value 1200 and 4600. What is EA of the memory operand in each of the following instructions?
   i) Load 20 (R_1), R_5
   ii) Move # 2000, R_5
   iii) Store R_5, 30 (R_1, R_2)
   iv) Add –(R_2), R_5
   v) Subtract (R_1) +, R_5. **10 Marks)**

   b. Write assembly language program to find sum of N numbers. **(06Marks)**

   c. What are assembler directives? Explain any two directives with examples. **(04Marks)**

5 a. What are the two different I/O techniques in which CPU is directly involved in data transfer? **(12 Marks)**

   b. Explain how DMA transfer will improve the data transfer rate in a computer. **(08 Marks)**

6 a. With neat diagram, explain the internal organization of 2M x 8 dynamic memory chip. **(10 Marks)**

   b. Discuss synchronous DRAM with its block diagram. **(10 Marks)**

7 a. Explain Booth's algorithm to multiply two signed numbers with example (+13) x (-6). **(10 Marks)**

   b. Explain restoring binary division with diagram. **(10 Marks)**

8 Write short notes on:
   a. Multiple bus organization
   b. Virtual memory
   c. IEEE floating point standard
   d. Basic instruction notation and types. **(20 Marks)**

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07MCA13

First Semester MCA Degree Examination, May/June 2010
Fundamentals of Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Carry out the following conversion :
i) $(347)_8$ to ( )$_{16}$
ii) $(29.35)_{10}$ to ( )$_2$
iii) $(1010111101.1100)_2$ to ( )$_{16}$. **(06 Marks)**

b. Why NAND and NOR gates are called as universal gates? Realise AND, OR, NOT and EX-OR gates using NAND gate. **(08 Marks)**

c. Write truth table and expression for output of a three input NOR gate and three input EX-OR gate. **(06 Marks)**

2 a. Construct a logic diagram, to implement the Boolean function $Y = \overline{P} \cdot Q + \overline{RS} + \overline{Q} \cdot S$, using two input gates only. (AND, OR, NOT, etc). **(05 Marks)**

b. Simplify the following logic expression using Karnaugh map
$f(w,x,y,z) = \overline{w}\overline{x}\overline{y}\overline{z} + \overline{w}\overline{x}\overline{y}z + w\overline{x}\overline{y}\overline{z} + w\overline{x}\overline{y}z + wx\overline{y}z + wxyz$. **(06 Marks)**

c. Explain with a block diagram and an example, working of a binary multiplier using repeated addition. **(09 Marks)**

3 a. Explain with a neat diagram, inter connection structure of processor and main memory. **(08 Marks)**

b. Explain the basic performance equation used for measuring performance of a computer. **(04 Marks)**

c. What do you mean by the byte addressable memory? Explain with an example. Explain the little endian assignment, with an example. **(08 Marks)**

4 a. What is meant by the addressing mode? Explain any four addressing modes, with an example for each. **(09 Marks)**

b. What are the assembler directives? How are they different from instructions? Explain any two assembler directives. **(05 Marks)**

c. Differentiate between the memory mapped I/O and I/O mapped I/O. **(06 Marks)**

5 a. What do you mean by interrupt driven data transfer? Explain in detail, the sequence of events that occur during this type of data transfer. **(08 Marks)**

b. What is DMA? List and explain the different ways in which data transfer can be done using DMA. **(06 Marks)**

c. What is bus arbitration? Explain any one method of arbitration, in brief. **(06 Marks)**

6 a. Give the organization of a 4M bit chip which uses 512 K × 8 as a module. Calculate number of address and data lines required. **(07 Marks)**

b. Explain the memory hierarchy, with reference to speed, size and cost. **(05 Marks)**

c. Explain with a diagram, how the virtual address is translated to physical address while using virtual memory. **(08 Marks)**

7 a. Explain the design and working of a bit carry look ahead adder. Explain how the carry look ahead logic makes this operation fast. **(08 Marks)**

b. Explain Booth's algorithm for signed number multiplication, with an example. **(07 Marks)**

c. Carry out division (-8) divided by (+5) showing all the intermediate steps clearly. **(05 Marks)**

8 Write short notes on :

a. 2's complement address/subtractors

b. Instruction execution and straight line sequencing

c. Synchronous bus

d. Cache mapping functions **(20 Marks)**

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